REMARKS

Status of the Claims

Upon entry of the amendment above, claims 20-46 will be pending, claims 20, 21, 022, and 29 being independent.

Summary of the Office Action

Claims 1-19 are rejected under 35 USC §102(e) as being anticipated by KISHIMURA (U.S. Patent Application Publication 2002/0097405).

Claims 1-19 are rejected under 35 USC §103(a) as being unpatentable over KISHIMURA in view of WISE et al. (U.S. Patent No. 6,821,865, hereafter "WISE").

Response to the Office Action

A. Summary of the Amendment

1. Specification

Attached is a substitute specification (both clean and marked-up versions), whereby section headings have been added, as well as changes of a "cosmetic" nature.

2. Claims

Original claims 1-19 have been canceled in favor of new claims 20-46, of which claims 20, 21, 22, and 29 are independent.

New claims 20-38 relate to original claims 1-19, with clarifying amendments.

No prohibited new matter has been introduced into the disclosure via the substitute specification or amendments to the claims.

B. Request for Withdrawal of Rejections Based Upon KISHIMURA, Alone or in Combination with WISE

Applicant respectfully requests reconsideration and withdrawal of the rejections that are based upon KISHIMURA, whether considered alone or in combination with WISE, at least for the following reasons.

Applicant has two main objections to the rejections. KISHIMURA is cited as anticipating Applicant's invention. A certain passage from WISE, a second document, is identified, viz., column 2, lines 53 to 55 of WISE, as shown below:

> Referring to FIG. **2**, a cross-sectional view of a portion of a partially processed IC is shown. As shown, a substrate **203** is provided. The substrate comprises, for example, silicon. Other types of semiconductor substrates such as gallium arsenide, germanium, silicon on insulator (SOI), or other semiconductor materials are also useful. The substrate, in one embodiment, includes a plurality of services such as trench capacitors of memory cells (not shown) in the array region of the substrate. Providing a substrate prepared with other types of devices is also useful. The devices may be formed at various intermediate points in the process, depending on the types of devices.

This passage is referred to in the rejection of claim 1 for obviousness (i.e., under USC §103(a); see Item 4, page 9 of the Office action, bottom paragraph). This passage is not cited in the rejection of independent claims 1, 2 and 3 for anticipation, but approximately in the middle of the third page of the reasons for the obviousness rejection, the examiner explains that one of ordinary skill in the art would well understand the semiconductor wafer of KISHIMURA is the silicon on insulator (SOI) device that Applicant claims. Therefore, concludes that Applicant's invention lacks novelty.

When comparing Kishimura properly, this is not the only distinction that KISHIMURA has with respect to Applicant's claims 1, 2, 3, and 10 (now claims 20, 21, 22, and 29).

The claims have to be distinguished in that respect, as we are claiming a test structure in claim 1 (new claim 20). The other independent claims 2, 3, and 10 (new claims 21, 22) are method claims.

The test structure identifys the SOI wafer as such, lines 1 to 2 of claim 20. The test structure is not used for this device, ***but is in this device***. It is therefore part of the SOI wafer. The claim language that further enhances this is in line 2, as the test structure is now explicitly mentioned to be in the SOI device.

Applicant submits that this was evident from line 1 of original claim 1, but also other amendments had been made to the claim, to enhance the understanding that the trenches have widths, and each island that is provided has another trench width than an island next to it. This is properly shown in Applicant's FIGS. 1a and 1b, depicted on the left-hand side below.

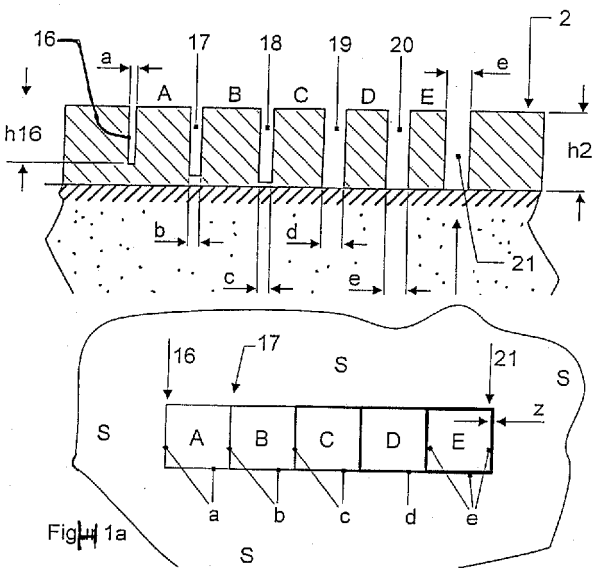
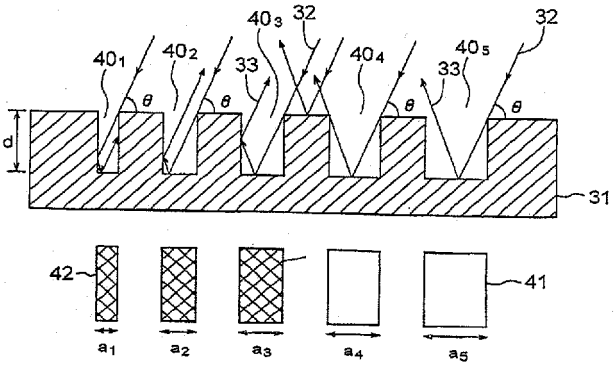


Fig. 1a

FIG. 3



When comparing KISHIMURA, FIG. 3 has to be interpreted properly. In the upper portion of this figure, a section is shown and in the lower portion, a view from top. Applicant's FIGS. 1a and 1b are reversed. Applicant has depicted his figures next to the KISHIMURA figures above in the same order, in that a section in the upper view and a view from top are shown in the lower picture. Taking the lower view of FIG. 1a of Applicant's invention as claimed, trenches a, b, c, d, e, ***all of which surround islands***. In the vertical section, the trenches are seen as lines; similar to the upper portion of FIG. 3 of KISHIMURA, but a view from the top is different.

A view from the top shows just rectangular gaps or holes in KISHIMURA. These gaps or holes are called trenches 40, page 2, paragraph [0030], forming dark images 42 for trenches with smaller width and bright images 41 for trenches with medium and larger width. So the

widths of these trenches change stepwise and increase, but KISHIMURA does not have islands that are surrounded by trenches, as Applicant claims.

The figure is just one example and a representation of what Applicant claims, but the claim under test of the examiner had effectively surrounding trenches and had common portions of these trenches between two islands (A, B) having an increased width. This is the trench width b between islands A and B. The trench width c is between islands B and C.

No such surrounding trenches can be seen in FIG. 3 of KISHIMURA. Also, FIG. 8 of KISHIMURA does not show these surrounding trenches, but has holes and does not show islands.

The whole test structure appears to be different, and Applicant has presented a structural distinction in the wording of previous claim 1 (now in claim 20), which was before the Examiner when the claim was rejected for anticipation.

New claim 20, an amended version of prior claim 1, enhances this and identifies the portion of the surrounding trench to be ***a sharing a portion*** of the next surrounding trench, which was in the second group of features already evident from previous claim 1. Applicant also identifies that his isolation trench that is to be measured or compared is ***away from the test structure***, as it is not part of the test structure. This was in the claim previously and is now more distinctly recited in claim 20. Applicant refers to this as the "certain trench width" which is to be compared to all the other trench widths that have increasing sizes from one island to the next. This is the wording and the language of claim 20 and this wording and the language distinguish over KISHIMURA.

To summarize this in small steps: Applicant has at least two islands in his claim 20. KISHIMURA does not have a single island. The island in Applicant's claim language is defined as contained within a surrounding trench. KISHIMURA does not have a surrounding trench. Consequently, no island is present.

Applicant has a common portion of two surrounding trenches. These surrounding trenches are "neighboring." The common portion has the width of the wider trench. This is not disclosed by KISHIMURA, but it is contained in the claim language of Applicant's claim 20.

The novelty rejection fails and, therefore, should be withdrawn. This is independent of an eventual discussion, whether an SOI wafer is implicitly contained in the language that WISE uses. As long as KISHIMURA does not use this interpretation, the novelty rejection fails, as one cannot adopt the terminology of a different prior art piece into the terminology of a primary prior art piece.

KISHIMURA is silent with respect to the underlying isolation (= insulation) layer between the substrate and the active portion of the wafer. This is not explicitly contained in Applicant's claim 20, but it is implicitly understood by one skilled in the art that something needs to be etched ***down to the isolation layer***, and only this device is then called an SOI device; see FIG. 2 and the general description on page 3 of the translation (of the underlying PCT international application), second paragraph, now paragraph [0014] of the attached substitute specification. When there is no isolation layer, no isolation trenches are needed and no bottom end can be reached that actually is the isolation layer. When the isolation trenches having a smaller depth than the active layer is thick (the height h2), all the measurement would not give any sense. Thus, one of ordinary skill, when applying plural measurement tests according to claims 21, 22, or 29 and using electrical pass test s, understands that something isolating must be there.

A general wafer, or as the examiner says, a "semiconductor substrate" in the meaning of WISE, eventually comprises an isolation layer below the active layer and a substrate below said isolation layer. This is mentioned below in lines 53 to 55 of the passage identified above:

Referring to FIG. **2**, a cross-sectional view of a portion of a partially processed IC is shown. As shown, a substrate **203** is provided. The substrate comprises, for example, silicon. Other types of semiconductor substrates such as gallium arsenide, germanium, silicon on insulator (SOI), or other semiconductor materials are also useful. The substrate, in one embodiment, includes a plurality of services such as

This language, however, is not adopted by KISHIMURA, and it is not used in Applicant's claim. Applicant claims an SOI device (SOI-substrate). So all three languages must be kept separate.

In individual steps, the §102 rejection is not warranted with respect to claim 20. Claim 20 has a surrounding trench and islands. It has many islands, and the extracted picture of FIG. 3 and the views of FIGS. 8a, 8b of KISHIMURA do not have trenches surrounding islands for a test structure. The SOI wafer includes – together with the test structure – an SOI wafer which can be tested during etching. The etching with respect to a certain depth of an insulation trench in an active circuit has to be verified. This can be done ***during*** etching or it can be done ***after*** an etching, with respect to an achieved target depth. Providing such facility for measurement is novel. The measurement as such is claimed in the method claims 21, 22, and 29. The measurement is not yet attributed to the structure of claim 20 that only has the inherent facility or inherent property to be measured.

Claim 21 is novel, as it claims a row of successive islands, eventually being subject to a measurement. This measurement is the electric pass. KISHIMURA makes structure for doing image patterns; see page 1, paragraph [0014]. The measurement trenches mentioned at the end of that paragraph and the depths are for reflecting light and being either dark or light in a picture taken from them, see page 2, paragraph [0030]. Applicant's claim 21 has a row of successive islands and they provide measurement as pass measurement, named "electrical pass". This can be either one of claims 24 or 25. None of the electrical pass measurements is of optical nature.

Claim 22 distinguishes over KISHIMURA by having the test structure which now has islands. Either the measurement is done between islands, or the measurement is done between the substrate region and one island. The first group of features names the islands more distinctly.

The test structure is not devoid of any certain shape or structure. In previous claim 3, the islands were mentioned, but new claim 22 recites such islands even more distinctly. An island requires that material is away from a surrounding region, and there must be some gap or trench between the substrate region and the island. One would not call something an island that is surface connected to the surrounding substrate. Claim 22 then requires measurement of the test islands as given before and refers these measurements to the target depth or target width of a trench that is located outside and associated with an active region or an active circuit, or electrically insulating many active circuits in said SOI wafer.

Claim 29 is novel, as it contains all the features that were previously identified. Applicant has the test structure that is on the SOI wafer and allows verification of electrical pass either between regions (as islands) or between a region and a surrounding one. Each of these regions or islands is surrounded by a trench. Such trenches have different widths, at least in this portion, which is a common portion of two neighboring trenches, or two neighboring islands; see, e.g., page 8, fourth paragraph from the top of the original specification (paragraph [0041]), as supporting disclosure. Claim 29 also uses the electrical pass, and distinguishes over KISHIMURA in structure and use of structure (= method).

The idea behind claim 20 as test structure and claims 21, 22, and 29 as method using island test structures is nicely explained on page 2, bottom paragraph, and page 3, paragraphs 1 and 2, of Applicant's original specification (i.e., the English language translation of the underlying PCT application, now paragraphs [0012]-[0014] of the attached substitute specification). Applicant notes that both types of measurement can be performed, firstly an online measurement by checking continuously the state of etching. In the alternative, Applicant can use a verification of an already etched device, and testing this for proper etching. Both methods are available with a structure of claim 20.

The claims not specifically mentioned above, are believed to be allowable at least for reasons set forth with regard to claims from which they depend, directly or indirectly.

CONCLUSION

The grounds of rejection advanced in the Office action have been addressed and are believed to be overcome. Reconsideration and allowance are respectfully requested in view of the amendment and remarks above.

Payment is being made herewith for an extension of time for three months and for extra claims. However, the Commissioner is authorized to charge any fee required for acceptance of this reply as timely and/or complete to Deposit Account No. 19-0089.

Any comments or questions concerning this application can be directed to the undersigned at the telephone number, fax number, or e-mail address given below.

Respectfully submitted,
Ralf LERNER

Reg No 32,674

Neil F. Greenblum
Reg. No. 28,394

December 1, 2008
GREENBLUM & BERNSTEIN, P.L.C.
1950 Roland Clarke Place
Reston, VA 20191
703-716-1191 (telephone)
703-716-1180 (fax)
jrowland@gbpatent.com